AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1-72. (cancelled)

73. (previously presented) An ESD protection device connected between a CMOS transistor and a pad for protecting said CMOS transistor from an overvoltage applied to said pad, said ESD protection element comprising:

a vertical bipolar transistor being formed on a semiconductor substrate for discharging accumulated electric charge of said pad from a surface layer of said semiconductor substrate towards a depth direction of said semiconductor substrate, wherein

said vertical bipolar transistor leads out collector electrodes through a collector-connection well and

said vertical bipolar transistor has a collector and a base formed in a same region using a same mask.

74. (previously presented) The ESD protection device according to claim 73, comprising plural said vertical bipolar transistors adjacent to each other.

75. (previously presented) The ESD protection device according to claim 74, wherein collector layers of said plural bipolar transistors are formed as a common layer.

76. (previously presented) A semiconductor integrated circuit, comprising:

said ESD protection device according to claim 73; and

a trigger device for switching said vertical bipolar transistor of said ESD protection device using an application of an overvoltage as a trigger, wherein

said trigger device comprises:

a diode having, in a joined state, a first conductive region formed simultaneously with said base of said vertical bipolar transistor on a surface of a semiconductor substrate and a second conductive region simultaneously formed with an emitter on a surface of said first conductive region.

77. (currently amended) The semiconductor integrated circuit according to claim [[75]] 76, wherein: in the diode of said trigger device; said first conductive region forms an anode and said second conductive region forms a cathode; and said semiconductor substrate of a first conductive type and said anode are insulated in said second conductive region simultaneously formed with said collector of said transistor.

78. (previously presented) The semiconductor integrated circuit according to claim 77, wherein, in said trigger device, said anode is connected with said base of said vertical bipolar transistor and said cathode is connected with said collector of said vertical bipolar transistor.

79. (previously presented) The semiconductor integrated circuit according to claim 78, wherein said base of said vertical bipolar transistor is connected with a ground terminal through a resistor.

80. (previously presented) The semiconductor integrated circuit according to claim 76, wherein said diode is a single diode or plural diodes connected in series; said overvoltage is a forward voltage for said diode; and breakdown is caused by energization.

81. (previously presented) The semiconductor integrated circuit according to claim 76, wherein:

said trigger device comprises a vertical bipolar transistor and a resistor;

said vertical bipolar transistor of said trigger device has a same structure as that of said vertical bipolar transistor of said ESD protection device, in which a semiconductor structure between a collector and a base forms a diode which breaks down by an overvoltage; and

said resistor is connected between said base and said ground of said vertical bipolar transistor forming said diode, which increases a base potential of said vertical bipolar transistor of said ESD protection device by a trigger electric current due to the breakdown by the overvoltage.

82. (previously presented) The semiconductor integrated circuit according to claim 81, wherein:

said trigger device comprises NPN type first and second vertical bipolar transistors which function as a diode;

said ESD protection device comprises NPN type third and fourth vertical bipolar transistors;

in said first and third vertical bipolar transistors, collectors are connected to said pad, bases are connected with each other, and emitters are connected to a ground terminal;

said first resistor is connected between said bases of said first and third vertical bipolar transistors and said ground terminal;

in said second and fourth vertical bipolar transistors, collectors are connected to an electric power source terminal, bases are connected with each other, and emitters are connected to said pad; and

said second resistor is connected between said bases of said second and fourth vertical bipolar transistors and said pad.

83. (previously presented) The semiconductor integrated circuit according to claim 82, wherein a collector layer of said first vertical bipolar transistor and that of said vertical bipolar transistor of said ESD device are simultaneously formed.

84. (previously presented) The semiconductor integrated circuit according to claim 82, wherein a collector layer of said first vertical bipolar transistor and that of said vertical bipolar transistor of said ESD device are formed as a common layer.

85. (previously presented) The semiconductor integrated circuit according to claim 81, wherein:

said vertical bipolar transistor of said trigger device comprises a dummy gate electrode for preventing said base and said emitter from being connected by silicide; and

said dummy gate electrode is connected with a ground terminal.